Aditya Narayan

Research interests

CPU microarchitecture design, Memory system design, Silicon-photonic networks, Performance and power modeling and analysis of manycore systems, Cross-layer modeling and optimization

Education

2016–present **Ph.D in Computer Engineering** — **Advisor:** Prof. Ayse Coskun
Boston University — Expected graduation: May 2021
Department of Electrical and Computer Engineering — GPA: 3.8/4.0

2012–2014 **Master of Science in Electrical Engineering**
University of Pennsylvania
Department of Electrical and Systems Engineering — GPA: 3.5/4.0

2008–2012 **Bachelor of Engineering with Honors in Electrical and Electronics Engineering**
Birla Institute of Technology & Science, Pilani, India
Department of Electrical and Electronics Engineering — GPA: 8.81/10.0

Research experience

Sept'16–present **Graduate Research Assistant**, *PeacLab*, Boston University, Boston, MA, USA.
Thesis: Energy management of 2.5D computing systems with silicon-photonic links
- Microarchitecture of a high-throughput optically-controlled phase change memory
- Thermally-aware system-management policies in 2.5D and 3D-integrated chips with silicon-photonic interconnects
- Page allocation of heap objects in heterogeneous memory architectures with HBM, DDR4, RLDRAM

March–Sept'18 **Research Intern**, *CEA-Leti*, Grenoble, France.
- Architectural performance and power model for a 2.5D-integrated chip with silicon-photonic interconnects
- Runtime energy management policy to reduce photonic power with minimal storage overheads

Industrial experience

June–Oct'19 **VLSI Full-Chip Timing and Design Intern**, *Intel Corporation*, Hudson, MA, USA.
- Static timing analysis for timing convergence of high-speed interconnect in multi-die (EMIB) server SoC
- Developed automation tool that custom routes a high-speed interconnect design, optimized for timing and power

2014–2016 **Electrical Engineer**, *High Energy Physics*, University of Pennsylvania, Philadelphia, PA, USA.
CERN ATLAS Inner Tracker (ITk) Strip ASICs Project
- RTL design of *Fast Cluster Finder* to determine position of subatomic particles passing through Si sensors
- Pre-emphasis driver circuit for high-speed communications with leakage current minimization

Jan–June'12 **Wifi System Intern**, *Cambridge Silicon Radio*, Bangalore, India.
- Automated the remote scheduling for Wi-Fi System tests

Technical skills

Coding skills

Programming Languages: x86 assembly, C, C++, Verilog, CUDA

Scripting Languages: Python, Shell, Tcl

Operating Systems: Linux, Unix, MacOS, Windows

Circuit Design CAD tools

Cadence tools: Virtuoso Schematic & Layout, RTL Compiler, Encounter, Liberate

Synopsys tools: Primetime, PrimePower, IC Compiler II, StarRC

Architectural Simulation tools

Gem5, Sniper, McPat, HotSpot, NVMain

Selected projects

Spring 2017 **A GPU-based Accelerator for PageRank (Language: C++, CUDA)**
Prof. Martin Herbordt
Parallelized version of PageRank algorithm on NVIDIA P100 GPU

Fall 2016 **FPGA Acceleration of DNA Sequence Mapping (Language: Verilog)**
Prof. Wenchao Li
Parallel Smith-Waterman algorithm for DNA sequence matching on a Zedboard Zynq FPGA

Fall 2013 **A Fully Pipelined Out-of-Order Processor Design using Dynamic Scheduling (Language: C++)**
Prof. Joseph Devietti
N-way superscalar machine with out-of-order execution based on Tomasulu's algorithm

Achievements

2018 Carnot Scholarship for research internship at CEA-Leti for March-Sept 2018

2018 2017/2018 Outstanding Graduate Teaching Assistant at Boston University

2017 A. Richard Newton Young Fellowship at 54th Design Automation Conference

2016 Distinguished Computer Engineering Fellowship at Boston University for the academic year 2016-17

Publications

Peer-reveiwed Journals:

2020 **A. Narayan**, Y. Thonnart, P. Vivet and A. Coskun "PROWAVES: Proactive Runtime Wavelength Selection for Energy-efficient Photonic NoCs" *IEEE Transactions on Computer-Aided Design (TCAD), 2020*

2020 A. Coskun, F. Eris, A. Joshi, A.B. Kahng, Y. Ma, **A. Narayan** and V. Srinivas. "Cross-Layer Co-Optimization of Network Design and Chiplet Placement in 2.5D Systems" In *IEEE TCAD, 2020*

2017 W. Lu, F. Anghinolfi, L. Cheng, J. N. Dewitt, J. Kaplon, P. Keener, **A. Narayan**, M. Newcomer and K. Swientek. "Development of the ABCStar front-end chip for the ATLAS Silicon Strip Upgrade" In *Journal of Instrumentation 12.04 (2017): C04017*

Conference Proceedings:

2021 **A. Narayan**, Y. Thonnart, P. Vivet, A. Joshi and A. K. Coskun. "OPCM: Optically-controlled Phase Change Memory" Submitted to *Symposium of High Performance Computer Architecture (HPCA), 2021 (Under review)*

2020 **A. Narayan**, A. Joshi and A. K. Coskun. "Bandwidth Allocation in Silicon-Photonic Networks Using Application Instrumentation" In *Proc. of IEEE High Performance Extreme Computing Conference (HPEC), Sept. 2020*

2020 **A. Narayan**, Y. Thonnart, P. Vivet, A. Joshi and A. K. Coskun. "System-level Evaluation of Chip-Scale Silicon Photonic Networks for Emerging Data-Intensive Applications" In *Proc. of Design, Automation and Test in Europe (DATE), March. 2020*

2020 Y. Thonnart, S. Bernabé, J. Charbonnier, C. Bernard, D. Coriat, C. Fuguet, P. Tissier, B. Charbonnier, S. Malhouitre, D. Saint-Patrice, M. Assous, **A. Narayan**, A. Coskun, D. Dutoit and P. Vivet. "POPSTAR: a Robust Modular Optical NoC Architecture for Chiplet-based 3D Integrated Systems", In *Proc. of DATE, March. 2020*

2019 **A. Narayan**, Y. Thonnart, P. Vivet, C. Fuguet and A. Coskun. "WAVES: Wavelength Selection for Power-Efficient 2.5D-Integrated Photonic NoCs" In *Proc. of DATE, March. 2019*

2018 **A. Narayan**, T. Zhang, S. Aga, S. Narayanasamy, A. Coskun. "MOCA: Memory Object Classification and Allocation in Heterogeneous Memory Systems" In *Proc. of International Parallel and Distributed Processing Symposium (IPDPS), May. 2018*

Workshop Talks and Posters:

2020 **A. Narayan**, Y. Thonnart, P. Vivet, A. Joshi and A. K. Coskun. "Energy-Efficient Photonic Networks for 2.5D manycore systems" *Poster presented at Design Automation Conference PhD Forum, 2019*

2019 **A. Narayan**, Y. Thonnart, P. Vivet and A. K. Coskun. "Power-efficient Photonic Network-on-chips via System-level Wavelength Optimization" In *Workshop on Silicon Photonics for High Performance Computing (SPHPC), 2019*

2019 **A. Narayan** and A. K. Coskun. "A System-Level Perspective on Silicon Photonic Network-on-Chips" In *International Workshop on Optical/Photonic Interconnects for Computing Systems (OPTICS), March 2019*